

Optimization of Phase Change RAM Write Performance for Large Memory Array

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Phase change memory (PCM) is widely considered to be a potential next-generation solid-state memory. The two main challenges associated with this technology are RESET current reduction and improving the write performance. Both write performance as well as energy consumption are dominated by the SET operation. For a given phase change material, optimizing the SET operation parameters is of utmost importance. In order to achieve a minimum SET timing, we first optimize the RESET state of the array. Then we employ a novel and effective method to derive a high speed SET pulse from the RESET current properties of the PCM array. As a starting point, the RESET operation is optimized by programming of the memory array with pulses of varying amplitude and width. A subsequent analysis of the resistance distributions shows that tail cells require a 60% larger RESET amplitude than the median cell. Optimum RESET resistance distributions are achieved with 1.4mA RESET current and 50ns pulse width.

The SET speed for individual cells is determined by the crystallization time of the amorphous to crystalline phase. A successful SET of the complete memory array requires that all cells are heated to their individual optimum crystallization temperature for a sufficient time. The difficulty is that for a given SET pulse length, there is a spread in the optimum pulse amplitude due to process variations in the array. To overcome those cell by cell variations, we propose a novel algorithm to derive the SET pulse amplitude directly from the RESET current distribution of the array. For this purpose, the RESET current distribution is divided into three segments and the SET amplitude is calculated as median RESET current for each segment multiplied by 0.4. The three resulting SET pulses are then combined to one decreasing cascade of pulses with equal duration.

A comparison of the optimized SET pulse to the best single SET pulse shows that the optimized SET pulse yields a better resistance distribution even with a 20% reduced SET time. The robustness of this new SET pulse with respect to RESET amplitude variations and cycling up to $8E6$ cycles is demonstrated based on 256kb memory arrays in 180nm technology with complex doped $Ge_2Sb_2Te_5$ in mushroom cell geometry.