

# Investigation of a new Three Bits Cell concept

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**Abstract**— New innovative electronics applications require larger memory capacity with decreasing memory array size. In this way, architectures implementing multi-bits or multi-level operations draw much attention because they proved to be one of the ways to reach this goal. In this paper, a Three Bits Cell concept, allowing 3 bits functionality, is investigated. This solution is obtained with multi-bits and multi-level memory combination. Such memory cell requires a perfect control of injection mechanisms. This paper presents cell design and injection mechanisms optimization. This cell is based on two floating gates architecture coupling with a middle channel

implant. The erasing operation is done by Fowler-Nordheim with sharp (FNSE) effect in the floating gates. This injection needs a precise process creating sharp on the floating gate. This sharp effect increases the tunneling electric field by a factor of 400 locally. Furthermore, a study is achieved with different doping characteristics to improve electron Band To Band Tunneling effect (eBTBT) used during writing operation. This study leads to an increase of the injection current, which is 10 times greater than a classical structure. The electrical characterizations of these mechanisms are performed to highlight the huge possibilities of this cell.